

WHAT IS CLAIMED IS:

- 1     1.     A memory device comprising:  
2             a plurality of pipeline stages for accessing data;  
3             a plurality of clock domains, each clock domain having circuitry controlled by a  
4     separate clock;  
5             a clock control circuit configured to selectively supply clock signals to the clock  
6     domains so that the clock domains are all activated in advance of, and corresponding  
7     to, when the clock domains are needed for a corresponding pipeline stage, all of the  
8     clock domains being activated sufficiently in advance so that a clock domain turn-on  
9     latency is transparent to a data access.
- 1     2.     The memory device of claim 1 wherein the clock domains comprise:  
2             a control circuit clock domain; and  
3             a data path stage clock domain.
- 1     3.     The memory device of claim 1 wherein the stages comprise:  
2             a RAS control stage connected to a first clock domain; and  
3             a CAS control stage connected to a second clock domain.
- 1     4.     The memory device of claim 1,  
2             a clock source, having at least two clock speeds, for providing clock signals to  
3     the plurality of clock domains;  
4             a clock controller configured to dynamically select a clock speed output by the  
5     clock source in accordance with a needed bandwidth of the interface.
- 1     5.     The memory device of claim 4 wherein one of the at least two clock speeds is  
2     a slow clock selected by the clock controller when needed bandwidth is determined by  
3     the clock controller to be below a predefined threshold, and the slow clock speed is  
4     slower than another one of the at least two clock speeds.
- 1     6.     The memory device of claim 4 wherein the at least two clock speeds includes a  
2     first clock speed and a second clock speed that is slower than the first clock speed,  
3     the clock controller monitors bus traffic on a memory bus and selects the first clock

4 speed when bus traffic on the memory bus exceeds a predefined threshold, and  
5 selects the second clock speed when bus traffic on the memory bus falls below the  
6 predefined threshold.

1 7. A memory device comprising:  
2 a plurality of pipeline control stages for accessing data;  
3 a plurality of clock domains, each clock domain being connected to one of the  
4 stages;  
5 a clock control circuit configured to selectively supply clock signals to the clock  
6 domains so that activation of one control stage automatically initiates activation of a  
7 subsequent control stage.

1 8. The memory device of claim 7 wherein a first clock domain includes a sense  
2 control circuit, the first clock domain automatically activating a second clock domain  
3 including transfer and close control circuits.

1 9. The memory device of claim 8 wherein a first clock domain includes a transfer  
2 write control circuit, the first clock domain automatically activating a second clock  
3 domain including a retire write control circuit.

1 10. A memory device comprising:  
2 a plurality of pipeline control stages for accessing data;  
3 a plurality of clock domains, each clock domain being connected to one of the  
4 stages;  
5 a clock control circuit configured to selectively supply clock signals to the clock  
6 domains so that activation of one control stage automatically initiates deactivation of a  
7 control stage not needed for a subsequent operation.

1 11. The memory device of claim 10 wherein a first clock domain includes a close  
2 operation control circuit, the first clock domain automatically deactivating a second  
3 clock domain including transfer and retire write control circuits.

1 12. A memory system comprising:  
2 a memory;

3           a memory interface;  
4           at least a portion of one of the memory and the memory interface having at  
5 least two clock speeds;  
6           a clock controller configured to dynamically select a clock speed in accordance  
7 with a needed bandwidth of the interface.

1   13.   The memory system of claim 12 wherein the clock controller comprises a  
2 programmed microprocessor.

1   14.   The memory system of claim 12 wherein one of the at least two clock speeds  
2 is a slow clock selected by the clock controller when needed bandwidth is determined  
3 by the clock controller to be below a predefined threshold; and the slow clock speed is  
4 slower than another one of the at least two clock speeds.

1   15.   The memory system of claim 12 wherein the at least two clock speeds includes  
2 a first clock speed and a second clock speed that is slower than the first clock speed,  
3 the clock controller monitors bus traffic on a memory bus and selects the first clock  
4 speed when bus traffic on the memory bus exceeds a predefined threshold, and  
5 selects the second clock speed when bus traffic on the memory bus falls below the  
6 predefined threshold.